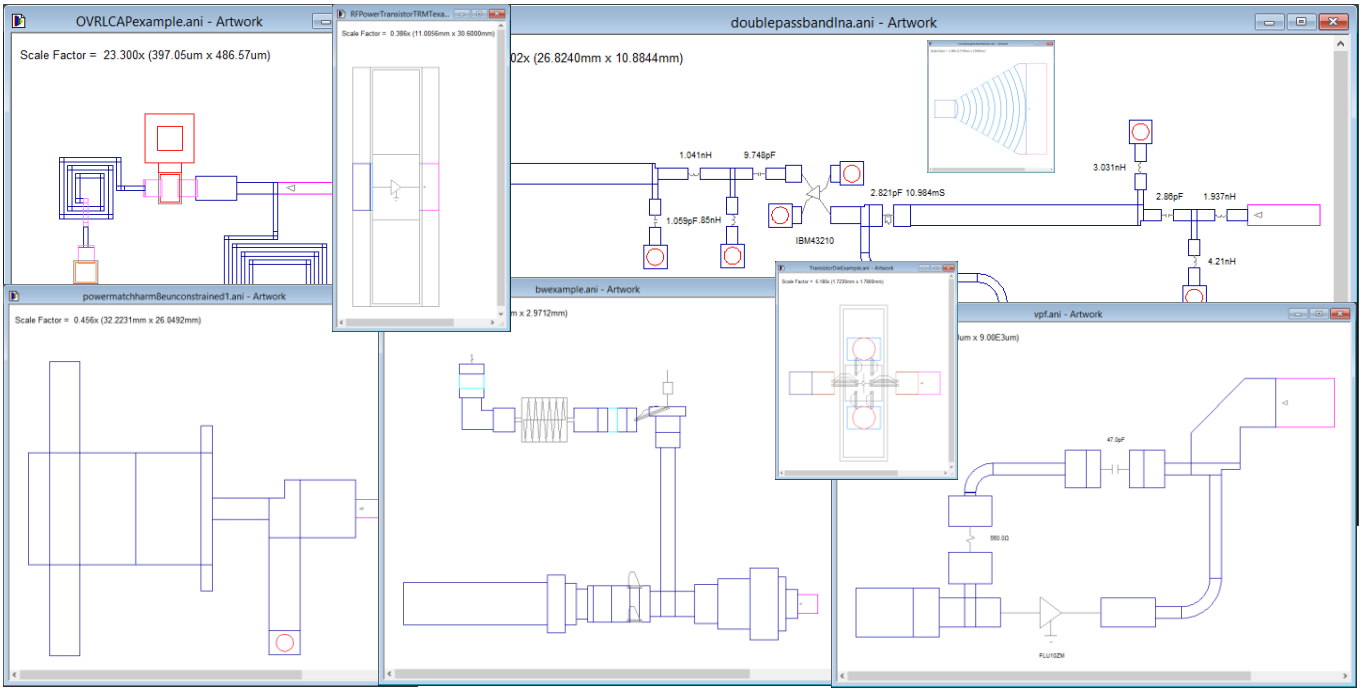
AMPSA ADW / IMW V10.4

REAL-WORLD SYNTHESIS DESIGN TECHNOLOGY FOR IMPEDANCE-MATCHING NETWORKS AND AMPLIFIERS



Products

The Impedance-Matching Wizard (Visual C^{++} 2015 Unicode MFC Program): Synthesizes high quality RF and microwave impedance-matching networks for user-defined impedance-matching problems up to artwork (microstrip) level. Harmonic control features are also provided (2nd and 3rd harmonics) in the IMW. These features are used when matching networks for high-efficiency amplifiers (Doherty, class F, inverted class F, etc.) are designed.

The Amplifier Design Wizard (Visual C^{++} 2015 Unicode MFC Program): Amplifier design and impedance-matching software. (The IMW is a subset of the ADW.) Small-signal, low-noise, power (class A and class B), high dynamic range amplifiers, high-efficiency amplifiers, as well as limiting amplifiers can be designed.

The ADW and IMW are the only commercial products which provide **real-world synthesis** capabilities to the designer. These products also **automate** many of the routine tasks typically performed by a designer.

Because of the **specialized structure** and the powerful **synthesis**, analysis, optimization, and **artwork** features implemented in the software, design cycles with the ADW are reduced to a fraction of the time previously required. The circuits designed are typically more robust (less sensitive) than those designed with other tools. This derives in part from the synthesis-based systematic searches implemented to ensure that the solution to each matching and modification problem is close to optimum.

Two design flows are provided in the ADW:

1. All the active work, including defining the specifications for the matching problems to be solved, is done in Microwave Office^{TM} or the Advanced Design System^{TM} and only the matching networks (with or without harmonic control) are designed with the Ampsa Wizards. A complete flow is provided for this in the ADW from synthesis, to fine tuning and introducing modifications in the matching network for biasing purposes, reducing discontinuity effects or replacing basic components with alternatives (inductor to spiral inductor or

solenoidal coil, etc.) to re-optimizing the matching network to restore its performance after the modifications made. The final matching network can be exported in various formats, including DXF, Sonnet Software® .son format and also as a Microwave Office™ script.

The parameters of the discontinuity models used in the ADW can be optimized to allow for easy adjustment of the network to provide the EM performance required. Only two EM simulations are usually required. The first simulation is used to adjust the parameters of the discontinuity models, after which it is re-optimized in the ADW and the second is used to verify that the performance is as required. Note that it may be necessary to reduce large steps in line width by introducing extra intermediate steps (tapering).

2. When linear cascade-type amplifiers are designed most of the work can be done in the ADW with linear models and boundary-line constraints on the *I*/*V*-plane, after which the designed amplifier can be exported for fine-tuning with non-linear models and further processing. The ADW design process usually starts with fitting linear ADW models to the **class-A or class-B** *S*-parameters of the transistors to be used at the required *dc* operating points (the operating point corresponding to the rated output power) and specifying the associated *I*/*V*-plane information. A **systematic approach** is then followed to design each stage of the amplifier, after which the completed design is optimized. The amplifier is then exported for fine-tuning and further processing. When the intrinsic load-line of a class-B stage is controlled, the required fundamental frequency and 2nd and 3rd harmonic intrinsic load impedance (and the associated external load) can be calculated for **class-F**, **continuous class-F**, inverted class-F and continuous inverted class-F performance. The required matching network can then be synthesized in the ADW, after which the performance of the stage can be evaluated in a harmonic balance simulator.

The ADW and the IMW are typically used as **front-ends** to one of the popular RF and microwave circuit simulators available on the market. The transition to these simulators are streamlined by the capability to export Microwave Office™ scripts, Sonnet Software® files (ADW only) and DXF files. Microwave Office scripts can be created for the schematic and the artwork, while Sonnet Software files can be created for the ADW artwork. The DXF files created for the artwork can be imported into CST Microwave Studio™ (a CST technology file is also created) and Momentum™.

Data Required

Transistor Data

When a class-A or class-B amplifier (linear amplifier) is designed with the ADW, ***S*-parameters** must be specified for the transistor(s) to be used at the relevant *dc* operating point(s) (that it, the *dc* conditions at the power level(s) of interest).- A small-signal model, the ***I*/*V*-curve load-line boundaries** (four boundary lines) and the *dc* operating point must be specified in order to control the maximum linear output power of a transistor. The **maximum linear output power** (pre-clipped output power) is usually a good estimate of P_{1dB} when a FET or a bipolar transistor is used.

If a small-signal model is not available at the required *dc* operating point, a model can be fitted in the Amplifier Design Wizard. The noise parameter modeling is also provided for (Fukui, Pucel and Pospieszalski noise models).

The small-signal model is used to **map** the **external** voltages of the transistor **to** the intrinsic output current and the **intrinsic** input and output voltages. The onset of **clipping** of the intrinsic current and/or voltage is used to predict the maximum linear output power of a transistor. In order to decide when the waveforms will clip an allowable load-line area on the intrinsic *I*/*V*-plane must be defined. In the ADW, the allowable area is defined by **four boundary lines** and the *dc* operating point. The information required for this purpose can be obtained from the dynamic (preferable) or static *I*/*V*-curves of the transistor. When *I*/*V*-curve information is not available, estimates can be used.

When a model for a transistor is created in the ADW, the default estimated value for the difference between the maximum linear output power and the saturated output power at the relevant *dc* operating point can be modified. This specification is used with the small-signal gain (load-line dependent) to define a **saturation curve**. This saturation curve is used to estimate the actual output power and the compression depth of each transistor. Note that because of the harmonic distortion it generally not advisable to drive a transistor too deep into **compression**. The compression depth can be controlled in the ADW.

Impedance-Matching Data

Impedance-matching problems must be specified in "**real-frequency**" format. The source and/or the load impedance may be complex, and the transducer power gain of the matching network can be controlled. In narrowband problems, control is also provided over the input or output impedance of the matching network at the 2nd and 3rd harmonic frequencies. A range of target reactance values can be specified at each harmonic frequency. Control over the resistance at the harmonics frequencies is also provided in order to minimize power generation at the harmonic frequencies.

A wide range of impedance-matching problems can be set up automatically for linear amplifiers by using the wizards provided in the ADW. When a non-linear amplifier is designed, load-pull information (based on measurements or non-linear simulations) is required in order to define the impedance-matching problems to be solved.

Note that the desired input or output impedance of each matching network to be designed, at any particular frequency, can be a **point** inside the Smith Chart (point-match), any point on the circumference of a Smith Chart circle (circle match), or any point in the area inside or outside such a **circle**. The circles of interest could be constant gain circles (inherent stability required) or constant noise figure circles, or circular approximations of areas defined by load-pull measurements (high efficiency and high power areas, etc.).

The fundamental frequency terminations for a matching network can be specified manually or data can be imported from Touchstone™ .s1p or .s2p files.

Main Features and Capabilities

Because of the **specialized structure** and the powerful real-world synthesis, analysis, optimization and artwork features implemented in the software, design cycles with the ADW and IMW are reduced to a fraction of the time previously required. The circuits designed are usually more robust (less sensitive) than those designed with other tools. This derives in part from the synthesis-based systematic searches implemented to ensure that the solution to each matching and modification problem is close to optimum (Forced solutions tend to be sensitive).

Accuracy is an important factor in a synthesis tool, especially at higher frequencies. Detailed **models** for parallel-plate capacitors, bond wires, solenoidal coils, hair-pin inductors, square spiral inductors, overlay capacitors, surface-mount resistors, capacitors and inductors, flip-chip resistors, etc. are, therefore, provided in the ADW. Many features were also implemented to allow components, as well as sub-circuits (like the individual matching networks) to be exported with minimal effort to EM simulation programs in order to ensure and verify accurate modeling. When an ADW sub-circuit has been refined in one of these EM tools, its ***S*-parameters** can be imported into the ADW to replace the original ADW sub-circuit. This is usually not required when accurate models are used for the components in the sub-circuit. Discrepancies may also indicate sensitivity, and if this is the case a different network should be designed.

The standard **microstrip models** used in the ADW and IMW are based on work done by Hammerstad and Jensen. Depending on the substrate height and the impedance levels, ADW microstrip or stripline circuits are usually adequate up to at least 12GHz. However, customization features were implemented to allow accurate results even at millimeter-wave frequencies, and also for low-impedance power amplifier circuits. These features are available in the professional versions of the IMW and the ADW.

Lumped-element models (MLIS, MLOS and MLSS commands) were added recently (based on work done by Gopinath and others) which allow accurate modeling of T-junctions and crosses up to much higher frequencies. The parameters in these models should be optimized by using a 2D or 3D EM simulator.

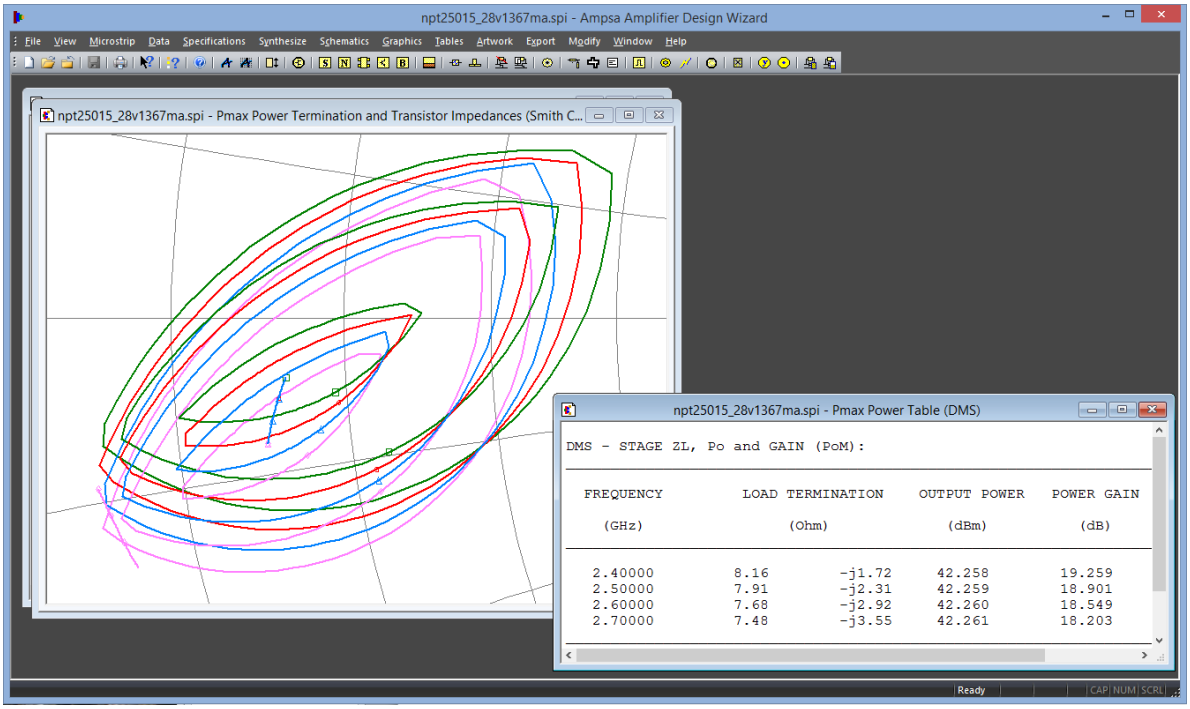
The circuits designed in the ADW or the IMW can be exported as **Microwave Office™ schematic scripts**, or in Super Compact™ or Touchstone™ nodal analysis format. The artwork and the schematics can also be exported in **DXF** or HPGL format. When the artwork is exported in DXF format a technology file is created to facilitate the import process when **CST's Microwave Studio™** is used. This file is used to extrude the different layers in the artwork at the correct heights with the correct thicknesses. The DXF layers are also mapped to the required CST materials and footprints are created for any bond wires used. In the ADW, the artwork can also be exported as a **Sonnet Software®** file (.son).

IMW Features and Capabilities

The Impedance-Matching Wizard synthesizes high quality RF and microwave impedance-matching networks up to artwork (microstrip) level. Pads and connecting lines, as well as parasitic inductance for capacitors and parasitic capacitance for inductors, can be specified for the networks to be synthesized. Shunt overlay capacitors and stepped main-line sections may also be used. Connections to the ground plane can be made with via holes or inductors (bond wires). A wizard is provided to assist with making the specifications for distributed or microstrip solutions. In

narrowband (less than an octave) problems, control over the input or output impedance of the matching network at the 2nd and 3rd harmonic frequencies is provided. Note that the components and the microstrip lines used are assumed to be lossless during synthesis.

Connecting lines can be added to the input and/or the output ports of a matching network in order to ensure that all the solutions obtained will effectively start and end with series elements. Short-circuited and open-ended stubs can also be added for biasing or harmonic control purposes.



A set of constant maximum linear output power contours was generated with the ADW for a power transistor. The load terminations required for maximum power are listed in the table.

Different types of networks can be synthesized with the Impedance-Matching Wizard. These include:

- **Lumped**-element networks.
- **Commensurate** distributed/microstrip networks (line lengths specified, widths used as variables).
- **Non-commensurate** distributed/microstrip networks (line widths specified, lengths used as variables).
- **Mixed** lumped/distributed networks (non-commensurate networks).

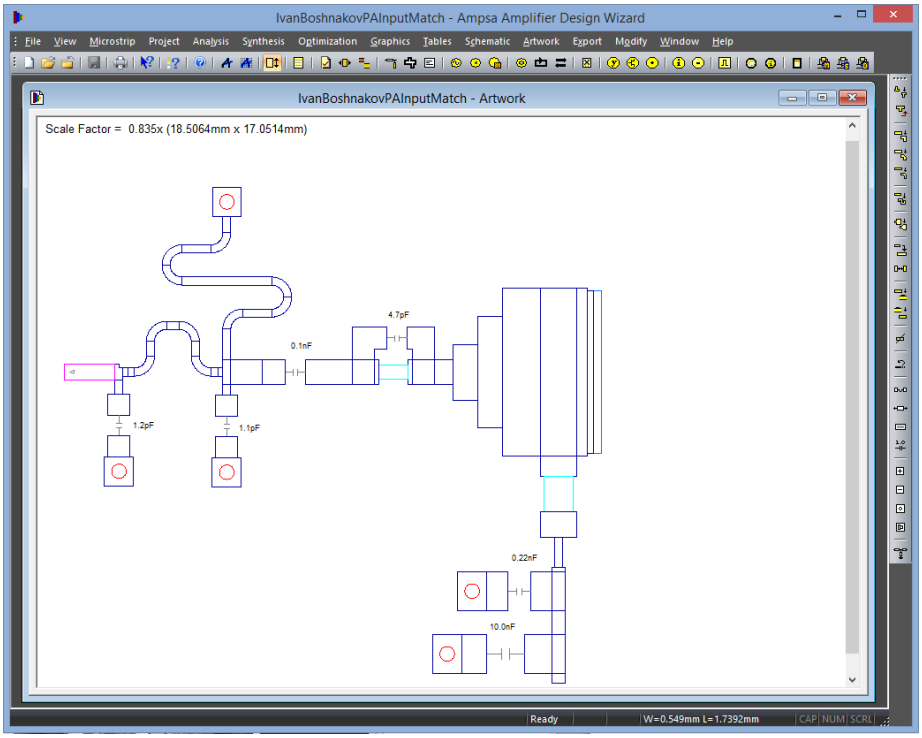
Synthesis is generally **over topologies** (topology independent). If required, the topologies can, however, be constrained to be of low-pass or high-pass form, to have no series capacitors, to be suitable for inter-stage biasing or to have no shunt inductors. The number of elements to be used must also be specified.

When commensurate networks are synthesized, all the line lengths are generally equal. This constraint has been relaxed to allow different lengths for the main-line sections, the open-ended stubs and the short-circuited stubs. It is a good idea to experiment with the line lengths when a new problem is solved. The length option can also be used to force the lengths of any stubs used to be electrically short. The stub impedance/susceptance will approximate that of the equivalent lumped component closely if this is done. This opens the possibility of replacing the stubs in the solutions synthesized with lumped components.

The lowest and highest characteristic impedances allowable in commensurate solutions must also be specified. Different constraints can also be imposed on the characteristic impedance values of the main-line sections, the open-ended stubs and the short-circuited stubs. The characteristic impedance values can also be left unconstrained initially. This is useful for establishing an appropriate range of characteristic impedance values for the problem to be solved. The information obtained should also be used when the substrate to be used is selected.

When non-commensurate solutions are synthesized, the characteristic impedances (lines widths) are fixed and must be specified by the user. High characteristic impedances are usually used for the main-line sections and any short-circuited stubs, while low characteristic impedances are usually used for any open-ended stubs. The characteristic

impedance (line widths) of the main-line sections can also be tapered (power matching problems). The initial and final characteristic impedance values to be used must then be specified by the user. Note that wide stubs can be replaced automatically with stepped main-line sections during synthesis.



An example of an ADW network designed to match the input of a power transistor.

When **mixed lumped/distributed networks** are synthesized, the non-commensurate distributed synthesis approach is followed, but the line lengths are reduced by using lumped inductors and/or capacitors when the required values are within the constraints specified. Shunt capacitors can also be replaced with overlay capacitors. Allowance is made for the associated line effect and via inductance when this option is selected. An extra connecting line can also be specified for shunt components. This option can be used to separate the shunt component pad from the main-line junction.

When microstrip solutions are required, the electrical parameters associated with the width and length specifications, as well as the associated T-junctions are also calculated and can be displayed. In order for the microstrip performance to closely approximate the desired electrical performance, the stub widths should be chosen to minimize the transformer and shunt susceptance loading effects associated with the T-junctions. Line losses should be taken into account when the minimum line width is specified.

Several solutions (usually with different topologies) are provided to each matching problem. When microstrip solutions are required, the **artwork** of each solution can also be displayed. Artwork editing capabilities are provided. When lines are curved or meanders are introduced, the physical line lengths are adjusted automatically to preserve the electrical performance.

The input and output impedance of each solution can be displayed graphically or in tabular form. When the harmonic impedances were controlled, the impedance at the harmonic frequencies can also be displayed.

A **worst-case tolerance analysis** is also done on the solutions provided. Preference should be given to insensitive solutions.

ADW Features and Capabilities

The Amplifier Design Wizard can be used to synthesize and optimize small-signal amplifiers, low-noise amplifiers, power amplifiers (class-A and class-B), as well as high dynamic range RF and microwave amplifiers (again class-A and class-B). The matching networks required in **high efficiency** power amplifiers (class-F, continuous class-F, inverted

class-F, Doherty, etc.) can also be designed in the ADW, but a third party tool is required for the simulation. The specifications for these matching networks can be set up by choosing to control the **intrinsic load line** in the ADW CIL wizard. Multiple passband amplifiers can also be designed in the ADW.

The networks designed with the ADW are **practical** and are adequate for **surface-mount** and **chip-and-wire** applications, as well as for **MMIC** applications. Single or double metallization, air-bridges, a capacitor dielectric layer and via holes can be used when MMIC circuits are designed in the ADW. Models for single-layer capacitors, square spiral inductors, single and double bond wires and solenoidal coils are also provided. The parameters in these models can be optimized by using a 2D or 3D EM simulator.

Power control in the Amplifier Design Wizard is based on an extension of the load-line approach commonly used at RF frequencies. By showing that it is actually the **intrinsic load impedance** that should be controlled and that the output power is inherently limited by clipping of either the intrinsic output voltage or the intrinsic output current in a transistor, Steve Cripps extended the usefulness of the RF load-line approach to microwave frequencies. This approach was generalized by the introduction of the **power parameters**. These parameters map the intrinsic output current and intrinsic input and output voltages of a transistor to the external voltages of the embedding circuit. This allows the intrinsic load line to be controlled (at the fundamental, as well as at harmonic frequencies) even when loading networks, impedance-matching networks or feedback is added to a transistor. Because the area without clipping is defined by four boundary lines, it is also possible to force the clipping to start on a specific boundary line or to prevent the clipping from starting on a specific boundary line.

It is sometimes not possible to solve a defined matching problem well (theoretical gain-bandwidth limitations). Frequency selective **resistive networks** can then be used to modify the problem appropriately. Double-section **modification networks** (feedback and/or loading networks added to a transistor) can be synthesized in the ADW to reduce gain-bandwidth constraints before a lossless matching network is synthesized. These modification networks can also serve to **level gain slopes** and to reduce or **remove stability problems** in amplifiers. They can also be designed to provide low VSWRs at the same time as a low noise figure and/or high output power.

Note that more optimization features are provided in the Impedance-Matching Module of the ADW than in the IMW. The solutions synthesized can be optimized in the results section of the Impedance-Matching Module in terms of the active performance targeted (That is, the power performance is optimized directly instead of optimizing the load reflection coefficients, etc.).

Amplifier design with the ADW is a **structured process**. The **stages** in an amplifier are **designed sequentially** (stage after stage). **Impedance-matching** and/or **modification** networks may be designed for each stage. Extraction of the "real-frequency" impedances (and the gain) required for the synthesis of the matching or modification networks is based on constant maximum linear power contours, constant gain circles and constant noise figure circles. The extraction is done in wizards and is automatic, but allows for user control. Optimization or optimization by re-synthesis is allowed at any stage during synthesis process and also when the basic design has been completed. This structured approach drastically improves the overall productivity of the design process. In addition to speeding up the process, it also leads to greater creativity and provides much more insight in the design than the standard optimization approach.

The **artwork** can be manipulated extensively in the ADW. This includes the following:

- Flipping stubs around.
- Adjusting the gap spacing or offsets vector used for a lumped component.
- Adjusting the dimensions of a line.
- Bending a line (optimum miter).
- Curving a line.
- Adding a meander in a line.
- Tapering a step junction.
- Closing any misaligned voltage-shunt feedback loop or series block loop (two cascade networks connected in parallel) automatically. A suitable component must be selected before the loop is closed.

When a line is bent or curved or a meander is introduced, the physical length of the line is adjusted to keep the electrical line length unchanged. Note that physical line lengths may also be adjusted to compensate for step junction, T-junction or cross junction discontinuity effects. The adjustments are made to get the performance of the microstrip circuit as close as possible to that of the electrical circuit.

Multiple substrates (up to nine) can be used in the ADW. **Artwork vectors** are used to define the connections to be made to transistors (die form or packaged).

One of the final steps in an ADW design cycle is usually to optimize the completed design in the Analysis

Module. (Note that, after the optimization, it is important to use the loop gain analysis feature to check the stability of each stage in the amplifier before the design is exported for further processing with another tool.) An **Optimization Wizard** is provided to set up the parameters of the error function to be used. Extensive control over the gain, the noise figure, the VSWRs, the stability factors, the maximum linear output power, the maximum linear power provided by each driver stage, and the maximum gain compression is provided. Error factors are also provided to prevent clipping of the intrinsic output voltage or current of a transistor on any of the four *I* / *V*-plane boundary lines allowed. It is also possible to control the amplification of the harmonics relative to the associated fundamental tone in wideband amplifiers. This is important in wideband amplifiers when low harmonic distortion is required.

The topology will usually not be changed when a circuit is optimized directly. The ADW Synthesis Wizards can, however, be used to re-synthesize any of the matching or modification networks in the amplifier. Note that the Two-port Command on the Schematic Toolbar can be used to replace any of the transistors used in the circuit with a different transistor, or the same transistor used at a different dc operating point, if necessary.

The **wizards** provided in the ADW are listed below, with a description of the function of each wizard.

General Impedance-Matching Wizard

The IIM, RMT, LMT and NOI commands can be activated by using this wizard. The different commands are described below:

IIM Command

This command can be used to set up an inter-stage impedance-matching problem. It can also be used to set up the matching problem associated with improving the input or the output match of the circuit.

The transducer power gain for the matching problem is set up automatically to level the overall transducer power gain of the circuit over the passband of interest. If a good match is required, the gain should be set to unity at each of the passband frequencies. This can be done in the impedance-matching section.

The source terminations for the left-hand side section of the circuit (section on the input side of the insertion point) are taken to be the actual source terminations of the circuit (as defined in the terminations block of the circuit file), while the load terminations for the right-hand side section are taken to be the actual load terminations.

RMT Command

The RMT command can also be used to set up an inter-stage impedance-matching problem, but instead of using the actual load terminations as load terminations for the section to the right of the insertion point (the output section), the terminations associated with the MAG (maximum available gain) of that section is used.

LMT Command

The LMT command is similar to the RMT command, but the input side of the section to the left of the insertion point (the input section) is terminated in its MAG terminations.

NOI Command

The NOI command is used to minimize the noise figure of the circuit section to the right of the insertion point (the output section). The circuit is assumed to be terminated on both sides as specified in the circuit file.

IVI Wizard

This wizard is used to set up an inter-stage impedance-matching problem to improve the input VSWR of the section to the left of the insertion point (input section) by mismatching its output impedance to the input impedance of the section to the right of the insertion point (output section). It can be used to improve the input VSWR of a low-noise amplifier. The gain of the amplifier can usually be leveled at the same time.

OVI Wizard

This wizard is similar to the IVI Wizard and is used to set up an inter-stage impedance-matching problem to improve the output VSWR of the section to the right of the insertion point (the output section) by mismatching its input impedance to the output impedance of the section to the left (the input section). As in the IVI case, the gain of the amplifier can usually be leveled at the same time.

CIL Wizard

This wizard is used to (re-)design an inter-stage or a load network to control the maximum linear output power (P_{out}), or the operating power gain (G_w) or the transducer power gain (G_T) of the section to the left (on the input side) of the insertion point. Note that information on the detailed performance (efficiency, gain, power, noise figure, stability factors, etc.) at each point on the contour is provided. If necessary, a point match can be enforced.

CIR Wizard

This wizard is used to (re-)design an inter-stage or a source network to control the noise figure (F), or the available power gain (G_a) or the transducer power gain (G_T) of the section to the right (on the output side) of the insertion point. Information on the detailed performance (efficiency, gain, power, noise figure, stability factors, etc.) at each point on the contour is provided. If necessary, a point match can be enforced.

MOT Wizard

This wizard is used to (re-)synthesize the modification network of a transistor and/or to replace the current transistor in an amplifier chain. It sets up the information required by the Device-Modification Module to insert a new stage (a transistor with its modification networks) at the insertion point.

Optimizing Impedance-Matching Networks in the ADW

The matching networks synthesized with the Impedance-Matching Wizard or the Impedance-Matching Module of the ADW can be processed further in the ADW. This processing includes comprehensive optimization of the solutions selected, adding components for biasing or *dc* blocking, replacing inductors with **square spiral inductors**, hair-pin inductors, solenoidal coils or bond wires (single or double geometrical bond wires are supported), and replacing capacitors with series or shunt **single-layer parallel-plate capacitors** (chip capacitors, MIM capacitors, etc.). Overlay capacitors with centered or offset via holes can also be used. When offset via holes are used in the overlay capacitors, one or two via holes can be used.

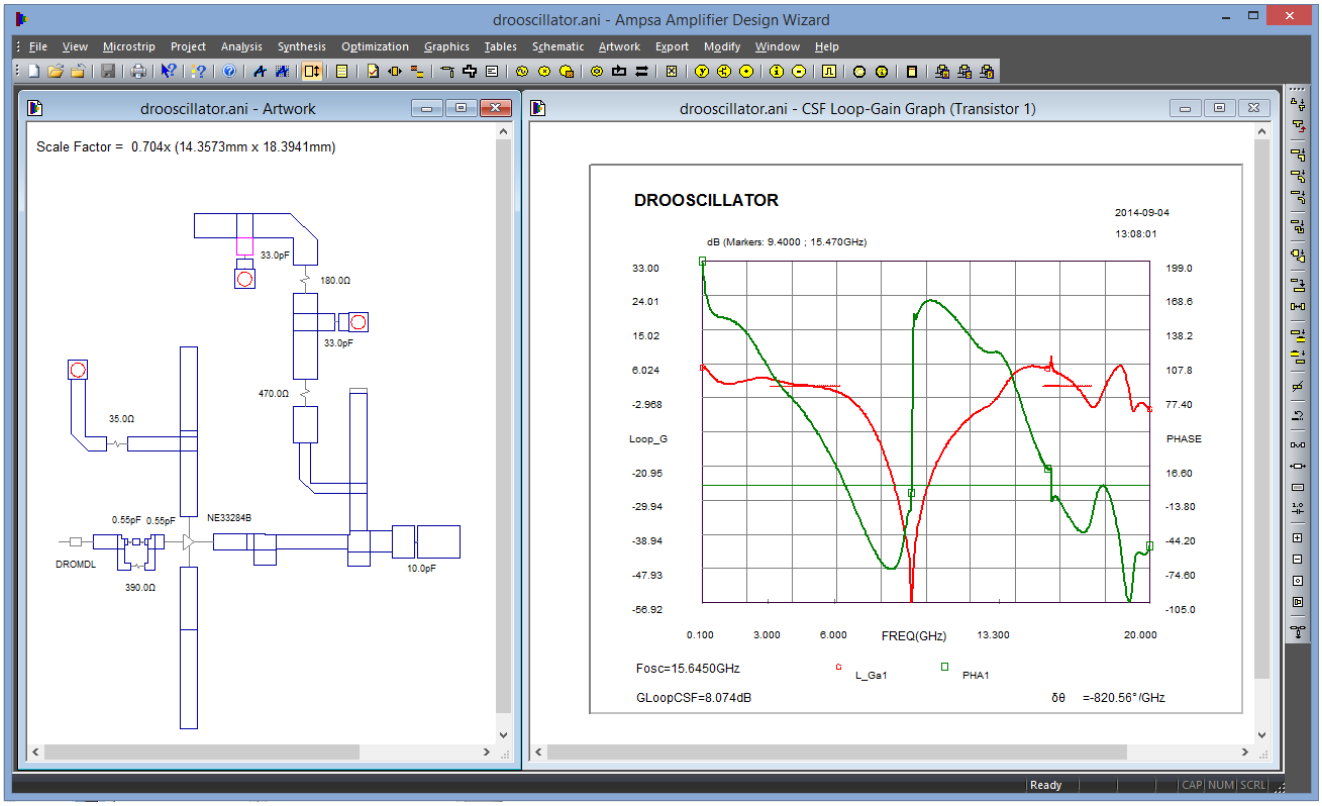
A special optimization option is provided in the ADW to optimize a matching network with an error function which is similar to the one used in the Impedance-Matching Module (harmonic control included). When this option is used, the reflection or the transducer power gain can be controlled. The reflection power gain should be used when the impedances presented to a transistor are important.

Stability Calculations

Modification networks are used in the ADW to stabilize each stage of an amplifier. In addition to the standard stability factors (Rollette and Sterne stability factors), the ADW **source stability factor** (SSF) and **load stability factor** (LSF) are also calculated when the stability is considered. These factors are similar to μ and μ-prime and are identical to these factors when the terminations of interest are equal to 50 Ω. When the termination of interest is complex, the complex termination is used instead of 50 Ω to calculate the SSF and LSF.

In addition to calculating the stability factors, the **loop gain** and **reflection gain** can also be calculated in the ADW. The reflection gain can be calculated at any point in the main cascade network. Feedback must have been applied to a transistor in order to calculate the loop gain. The gain and phase margins calculated provide important information on the relative stability of an amplifier stage. The effective resistance and reactance in each loop (the sum of the open-loop value and the feedback effect) should also be considered. Oscillations are only possible at frequencies where the effective

loop resistance is zero or negative. When this is the case the open loop and feedback reactance values must also have opposite signs in order for the loop reactance to cancel.



A Bode plot of the loop gain for a DRO oscillator is shown above.

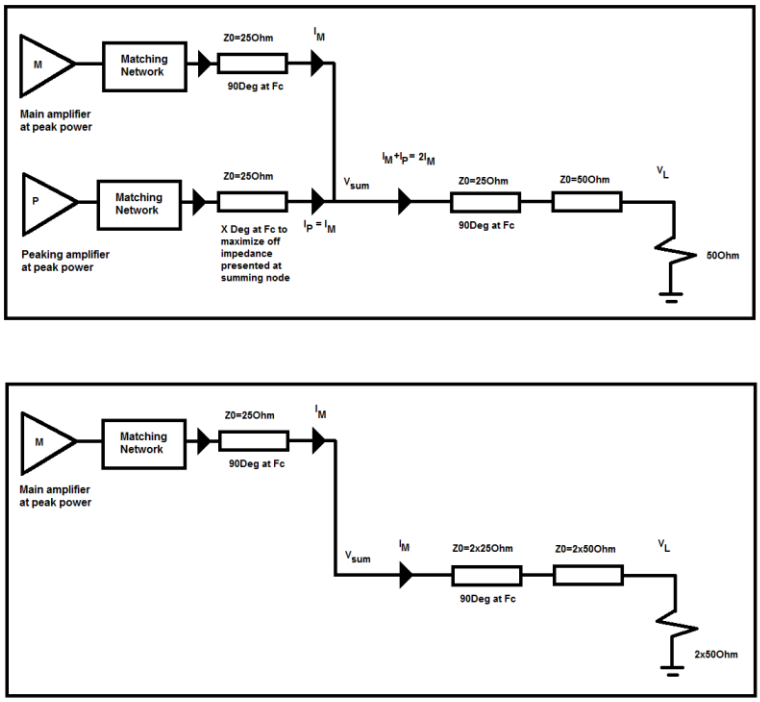
High-Efficiency Amplifiers

The harmonic control features implemented in the ADW and IMW are used to optimize the performance of class-B, continuous class-B, class-F, continuous-mode class-F, inverted class-F and continuous mode inverted class-F stages. The load-pull work required to set up these matching problems is best done in Microwave Office™ or ADS™, but good results can also be obtained by doing it the ADW (use the CIL wizard). If the ADW is used to obtain the load-pull information, the maximum linear output power (pre-clipped output power) is controlled. Because of the power parameters used in the ADW it is a simple matter to find the external impedance required to provide the intrinsic load-line targeted at the fundamental, as well as the harmonic frequencies.

Doherty Amplifiers

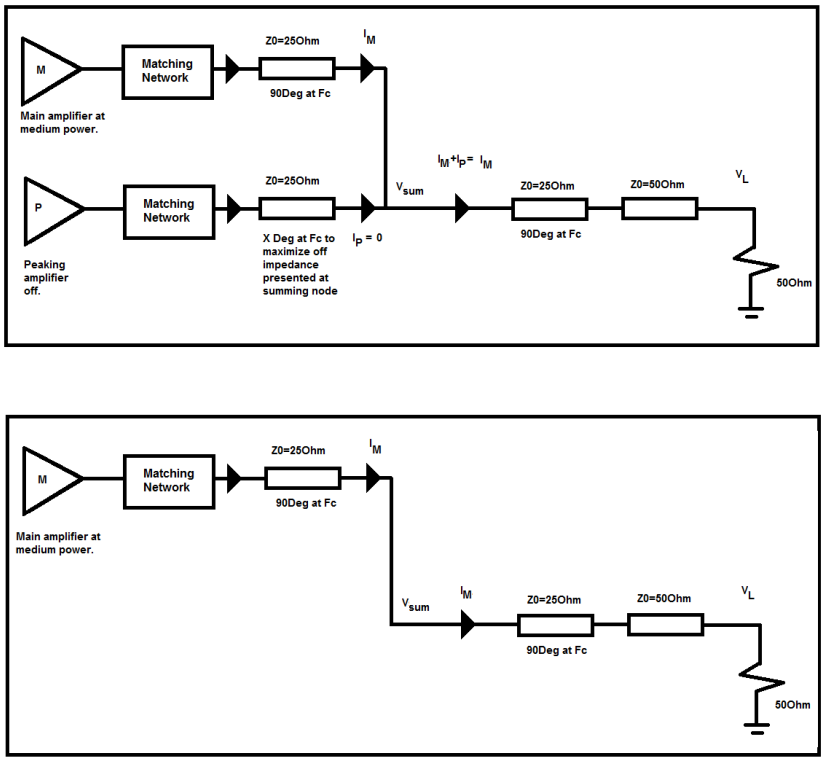
The load matching network for the main amplifier in a Doherty amplifier must **solve two impedance-matching problems at the same time** in order to maximize the power and efficiency at full power and at the back-off level targeted. The load-impedances for these two matching problems are different because of the Doherty principle, while the required input impedances must optimize the power and efficiency response at two different power levels. If a slight **offset** is used **in the frequencies** at which these two matching problems are defined, the specifications for the two problems can be merged in the ADW or IMW, and the two matching problems can then be treated as a single problem.

Single-ended equivalent circuits are used in the ADW to set up the two impedance-matching problems. In the back-off case the peaking amplifier is off and the loading effect of the peaking amplifier at the summing node can be assumed to be negligible or it can be estimated from a previous iteration. At peak power, the characteristic impedances of the lines on the load side of summing node and the actual load termination are impedance scaled to allow for the effect of the peaking amplifier on the current.

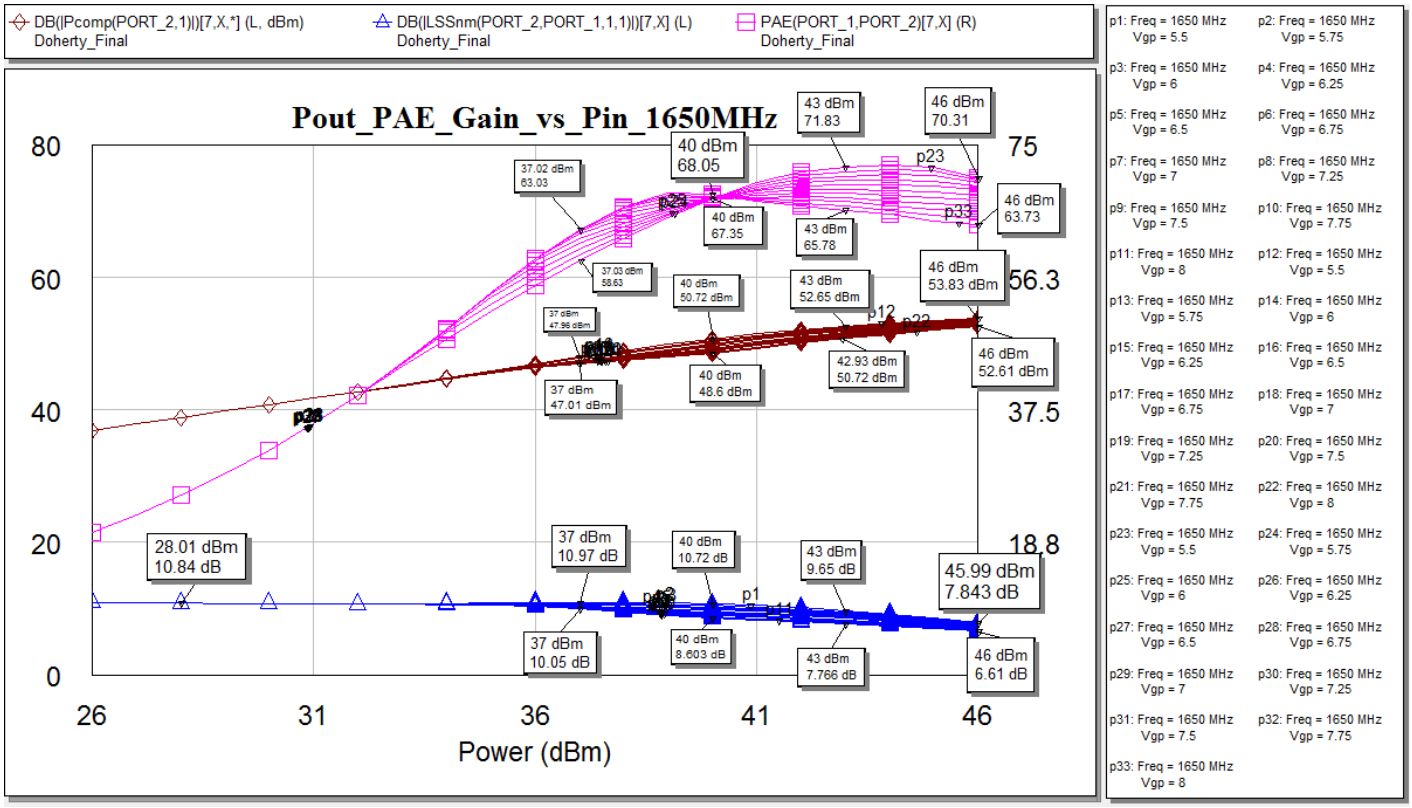


The single-ended ADW equivalent for a basic Doherty amplifier at peak power.

The load-pull work required to set up these matching problems is best done in Microwave Office™ or ADS™, but good results can also be obtained by doing it the ADW (use the CIL wizard; see the figure below). If the ADW is used to obtain the load-pull information, the maximum linear power is controlled and not the saturated output power. Tuning of the ADW networks synthesized may then be required to optimize the saturated performance.



The single-ended ADW equivalent for a basic Doherty amplifier at the back-off power level.



The performance of a Doherty amplifier synthesized in the ADW for the Cree CGH40120 GaN as simulated in Microwave Office™. The gate voltage on the peaking transistor (V_{gp}) was stepped from -5.5V to 8V. The load-pull work was also done in the ADW and was based on the *S*-parameters supplied in the data sheet.

Limiting Amplifiers

The **compression depth** of the different stages in a power amplifier can be estimated and controlled in the ADW. This capability allows for establishing proper power levels at the different points in an amplifier chain. It is also useful for ensuring that none of the transistors in the chain is over driven and also allows for indirect control over the harmonic and inter-modulation distortion generated by the different stages. Because of these capabilities, limiting amplifiers can also be designed with the ADW.

All of these features and capabilities combined make the ADW a formidable design tool for amplifier designers. It extends the power of the expert designer and assists novice amplifier designers to become experts. Many first-time-right ADW amplifiers have already been manufactured by Ampsa customers.

Platforms

The ADW and IMW are currently only supported on computers with Microsoft Windows™ operating systems (Windows XP™ and later). Windows 10™ is recommended.

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